REMARKS

This is intended as a full and complete response to the Office Action dated March 29, 2006, having a shortened statutory period for response set to expire on June 29, 2006. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-21 are pending in the application. Claims 1 and 3-21 remain pending following entry of this response. Claim 2 has been cancelled. Claims 1, 7, 15, and 18 have been amended to include the subject matter of cancelled Claim 2. Applicant submits that the amendments and new claims do not introduce new matter.

Claim Rejections - 35 USC § 102

Claims 1, 7, and 15 are rejected under 35 U.S.C. 102(b) as being fully anticipated by *Namekawa* (US Pat No. US 6115301 A). Applicant respectfully traverses this rejection. Claims 1, 7, and 15 have been amended to include the subject matter of cancelled claim 2. Applicant submits that the present rejection of Claims 1, 7, and 15 is moot in light of the amendment. Withdrawal of the rejection is respectfully requested.

Claim Rejections - 35 USC § 103

Claims 2-5, & 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Namekawa* (US Pat no. US 6115301 A) and further in view of *Arase* (US 5808945 A). Applicant respectfully traverses this rejection.

Claim 2 has been cancelled. Each of the independent claims have been amended to include the subject matter of Claim 2.

The Examiner bears the initial burden of establishing a *prima facie* case of obviousness. *See* MPEP § 2142. To establish a *prima facie* case of obviousness three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one ordinary skill in the art, to modify the reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Third, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *See* MPEP

§ 2143. The present rejection fails to establish at least the third criteria, as described below.

The pending claims each describe a test system or a test device. For example, Claim 1 refers to a memory module in a test system. Claim 7 refers to a test device for determining a repair solution for a memory module. Claim 15 refers to a test system including a connectable memory module and a test device. Claim 18 refers to a test system and a method for determining a repair solution for a memory module in the test system. The Examiner states that *Namekawa* describes a test device connectable to a memory module in Figure 1 and at Col. 3, Lines 20 to 65. *See Office Action dated March 29, 2006*, (hereinafter *First Office Action*), Pg. 3, Para. 3. The cited figure of *Namekawa* shows "an example of a semiconductor memory device". *Namekawa*, Col. 5, Lines 37-39. The cited section of *Namekawa* describes "a semiconductor memory device" which includes "a memory cell array in which a plurality of memory cells are arranged". The cited section and figure do not refer to a test system or a test device connectable to a memory module. Therefore, the cited sections of *Namekawa* do not teach the claim limitation asserted by the Examiner. Accordingly, Applicant submits that the *prima facie* case of obviousness has not been established. Withdrawal of the rejection is respectfully requested.

The pending claims each describe that "each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines" and "the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number".

The Examiner states that the claimed subject matter is described in *Arase* at Fig. 1, Fig. 3, Col. 3, Line 45 – Col. 4, Line 36, and Col. 5, Lines 10-65. *See Office Action*, Pg. 5, Para. 3. Fig. 1 of *Arase* is a view of a defective cell in units of main word lines. *Arase,* Col. 3, Lines 20-22. Fig. 3 of *Arase* is a view of redundancy given by a main bit line in a flash memory. *Arase*, Col. 3, Lines 30-31. Col. 3, Line 45 – Col. 4, Line 36 of *Arase* describes replacement of a defective cell by a redundant cell. *Arase,* Col. 3,

Lines 48-52. In the example, two regular main word lines are defective main word lines. *Arase,* Col. 4, Lines 19-20. The chip is saved by replacing the defective main word lines by a redundant main wordline. *Arase,* Col. 4, Lines 20-22. Col. 5, Lines 10-65 of *Arase* describe an example in which there is a defect in one memory cell in a group of regular sub bit line blocks. *Arase*, Col. 5, Lines 37-39. The chip is saved by replacing the defective main bit lines by redundant bit lines. *Arase*, Col. 5, Lines 40-43. Thus, the cited sections only describe replacement of a defective wordline by a redundant wordline and replacement of a defective bit line by a redundant bit line. The cited section does not refer to one or more replacement redundant groups which are selected from a redundant word line group "*if the defective memory areas that are addressable by a common word line group exceeds a first maximum number*" nor does the cited section refer to one or more replacement redundant groups which are selected from a redundant bit line group "*if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number*".

Therefore, the cited sections of *Arase* do not teach the claim limitation asserted by the Examiner. Accordingly, Applicant submits that the *prima facie* case of obviousness has not been established. Withdrawal of the rejection is respectfully requested.

Claims 6, 11, 12, & 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Namekawa* in view of *Arase*, and further in view of *Bemis* (US Pat no. 4692894 A). Claims 14, 16, & 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Namekawa* in view of *Sakata* (US PG-Pub no. 20010045581 A1). Claims 18-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Namekawa*, *Arase*, *Bemis*, and *Sakata* alone or in combination as stated above for the system and method as set forth in Claims 1-17. Applicant respectfully traverses the rejections. As described above, each of the dependent claims have been amended to include the subject matter of Claim 2. The rejection with respect to Claim 2 is believed to be overcome for the reasons provided above. Therefore, the claims are believed to be in condition for allowance, and allowance of the claims is respectfully requested.

Conclusion

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed.

Respectfully submitted, and
S-signed pursuant to 37 CFR 1.4,

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